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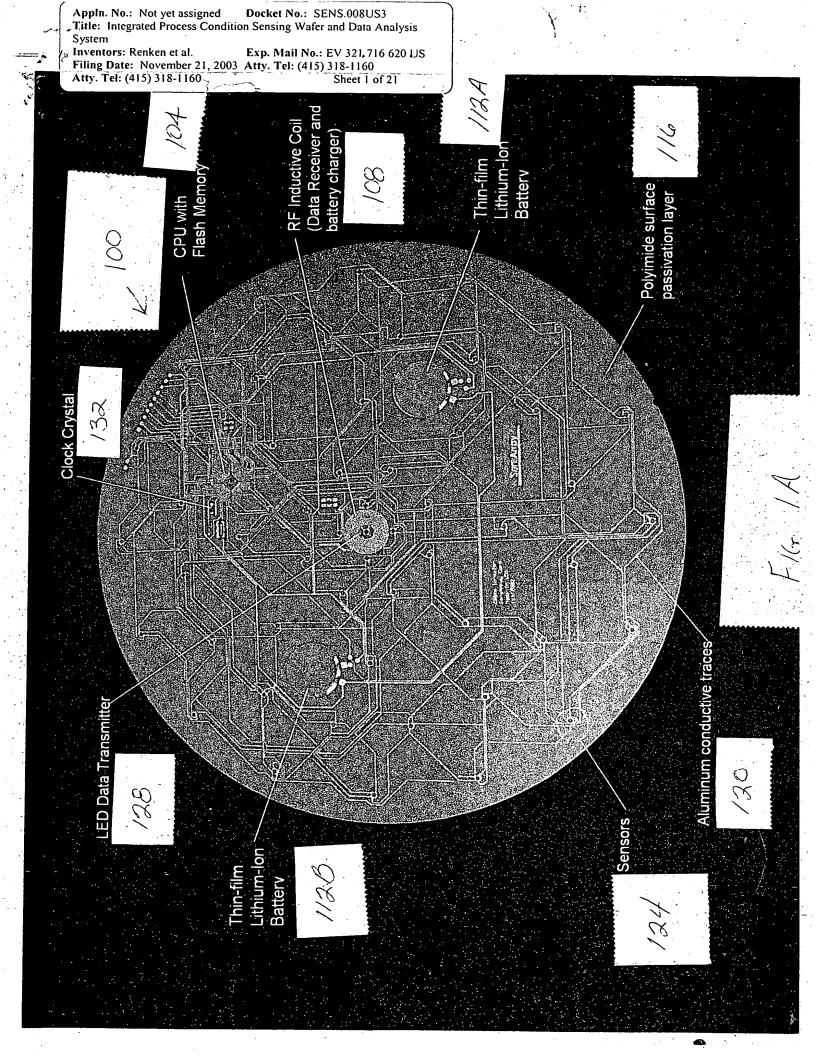
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System

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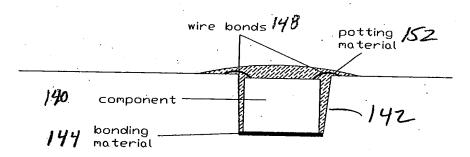
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sensor crystal osciallator CPU battery
124 /32 /04 112 resistor capacitor
113 115

Wafer 102

F16. 1B

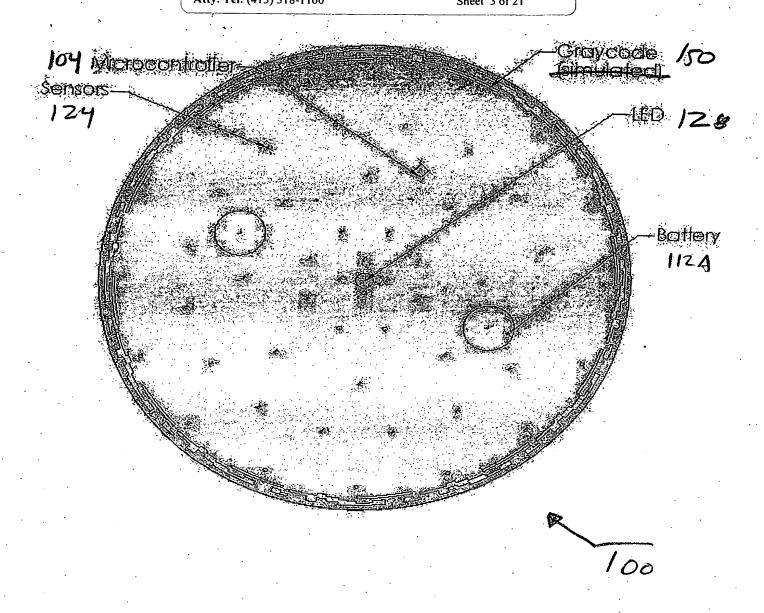
Components as imbedded in wafer (\*\* not to scale)



wafer/02

F/G./C
Detail of imbedded component (\*\*\* not to scale)

Appln. No.: Not yet assigned Docket No.: SENS.008US3
Title: Integrated Process Condition Sensing Wafer and Data Analysis System
Inventors: Renken et al. • Exp. Mail No.: EV 321 716 620 US
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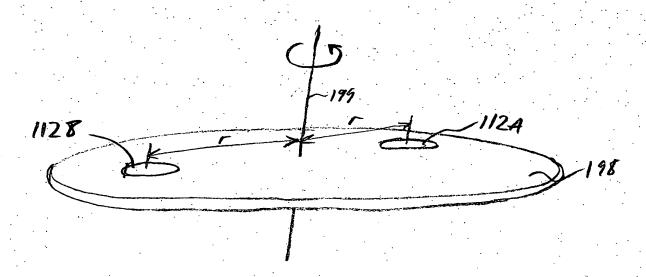
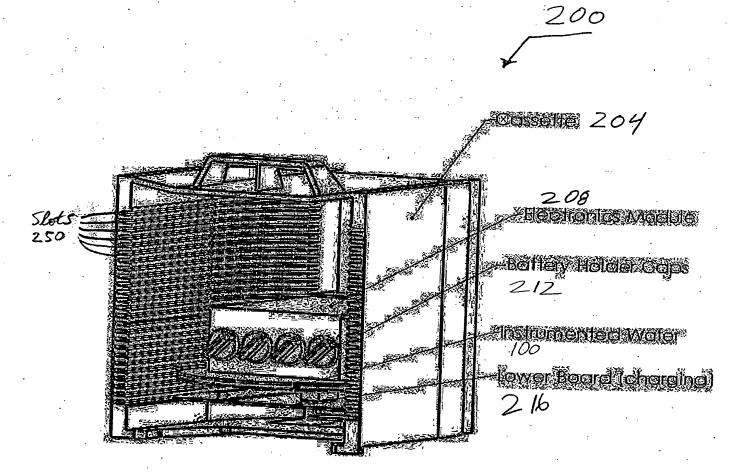


FIG. IE

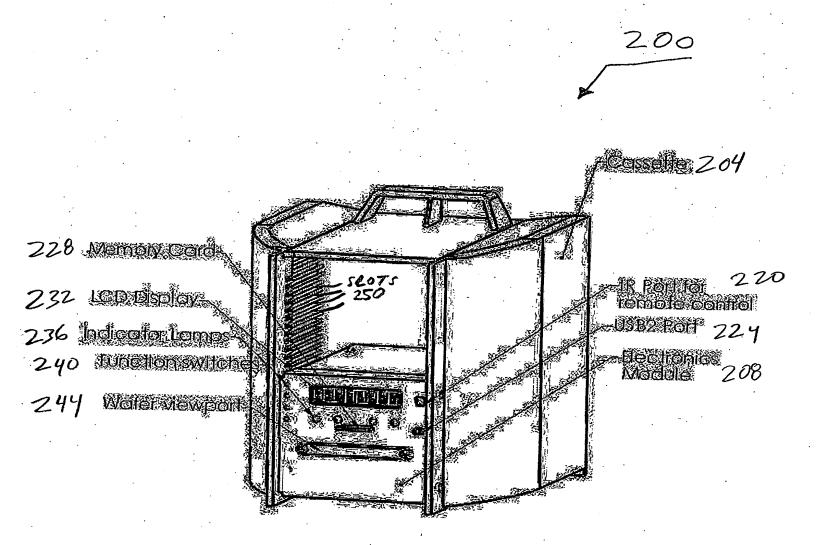
Inventors: Renken et al. • Exp. Mail No.: EV 321 716 620 US Filing Date: November 21, 2003 Atty. Tel: (415) 318-1160
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F16 2A

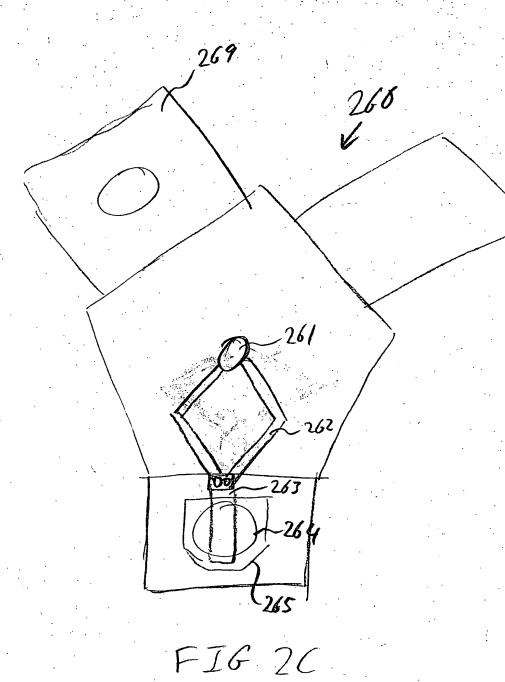
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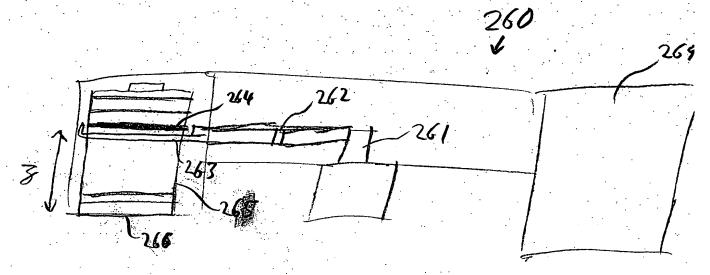
F1G. 2B

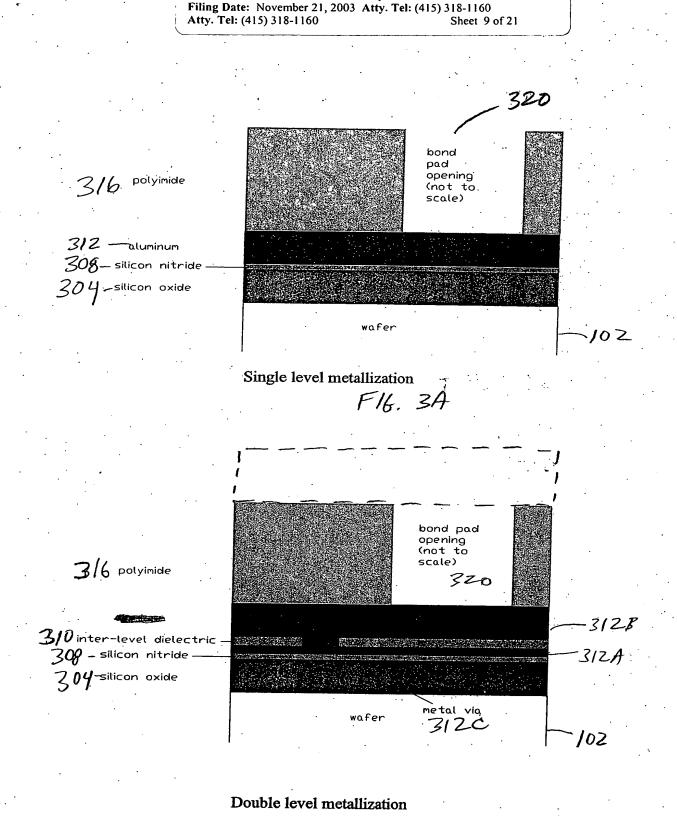
Inventors: Renken et al. \* Exp. Mail No.: EV 321 716 620 US Filing Date: November 21, 2003 Atty. Tel: (415) 318-1160
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System
Inventors: Renken et al.

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F16. 38

Appln. No.: Not yet assigned

Inventors: Renken et al.

Docket No.: SENS.008US3

Exp. Mail No.: EV 321 716 620 US

Title: Integrated Process Condition Sensing Wafer and Data Analysis

Appln. No.: Not yet assigned Docket No.: SENS.008US3 Title: Integrated Process Condition Sensing Wafer and Data Analysis Inventors: Renken et al. Exp. Mail No.: EV 321 716 620 US Filing Date: November 21, 2003 Atty. Tel: (415) 318-1160 Atty. Tel: (415) 318-1160 Sheet 10 of 21 FORM INSULATING LAYER 304 ON SUBSTRATE 102 FORM INSULATING 308 ON INSULATING LAMER 304 FORM CONDUCTIVE LATER 312 ON INSULATING LAYER 308 PATTERN AND ETCH ELECTRICAL TRACES IN/ON CONDUCTIVE LAYER 312 FORM PASSIVATION LAYER 316 CONDUTVE LAYER 312 FORM CAVITIES 142 FOZ COMPONENTS 140

412

420

424

432. PORM ADDITIONAL PASSIVATION LATER

( NOT SHOW!) OVER COMPONENTS

140 AND ETHER! LATERS

Title: Integrated Process Condition Sensing Wafer and Data Analysis System Inventors: Renken et al. Exp. Mail No.: EV 321 71 Filing Date: November 21, 2003 Atty. Tel: (415) 318-1160 Exp. Mail No.: EV 321 716 620 US Atty. Tel: (415) 318-1160 404 FORM INSULATING LAYER 304 ON SUBSTRATE 102 FORM INSULATING LAYER 308 ON INSULATING LATER FORM CONDUCTIVE LATER 312 A ON INSULATING LATER DIELECTRIC LAYER 310 CONDUCTIVE LAYER 3RA FORM OPENING FOR VIAS 3/2C IN DIELECTRIC LAYER 310 FORM CONOULTIVE LAYER 312B 415-VIAS 3/2C PATTER AND ETCH FLECTEICAL TRACS :416 IN CONDUCTIVE LAKERS 312 A,B 420 -432 SAME AS 14 F164A

Appln. No.: Not yet assigned

Docket No.: SENS.008US3

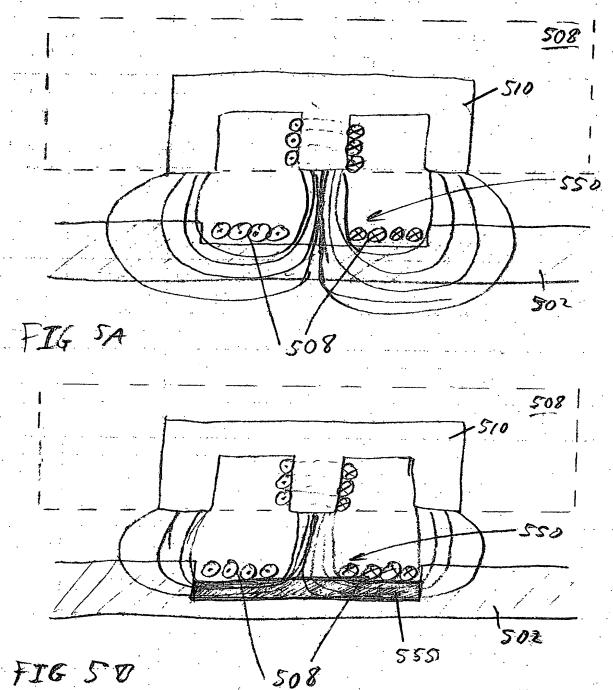
FORM ELECTRICAL AND CHEMICAL

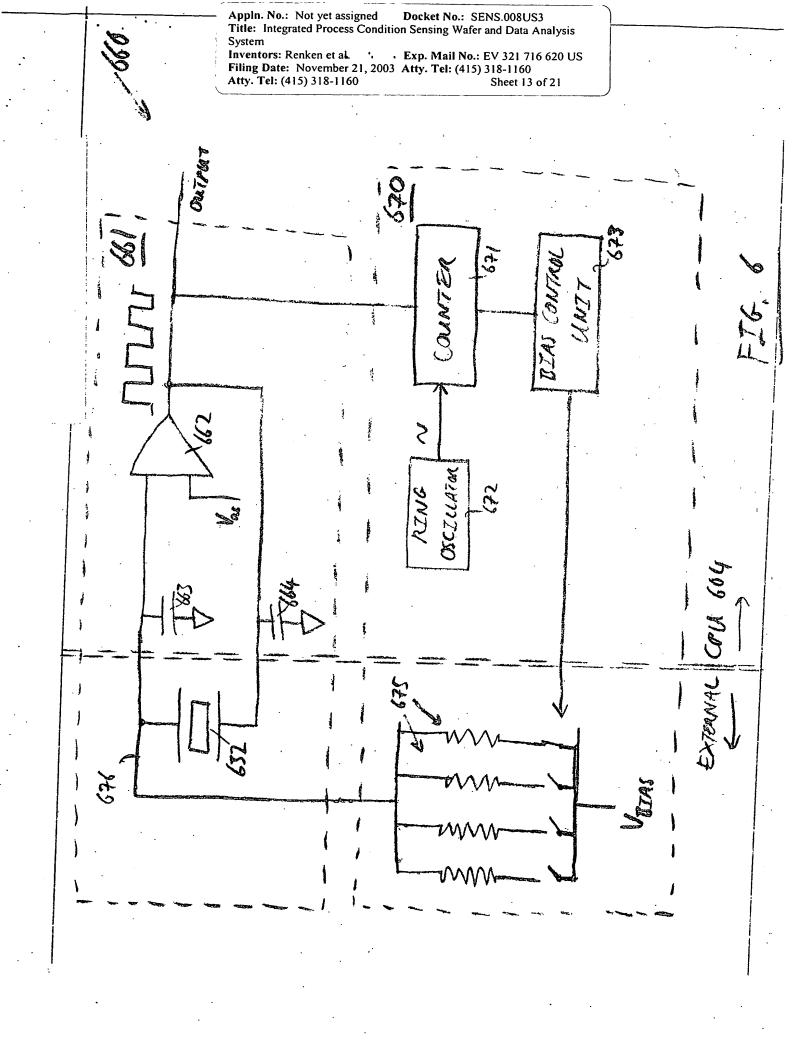
PROTECTIVE SHIELD LATER OVER

ADDITIONAL PASSIVATION LAYER

FIG. 48

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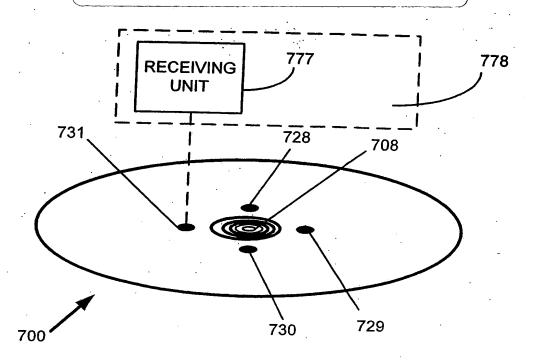


FIG. 7

Inventors: Renken et al.

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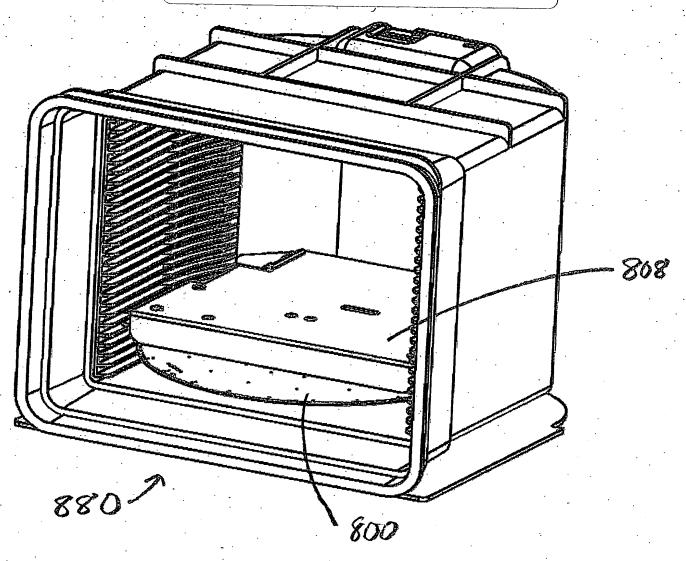
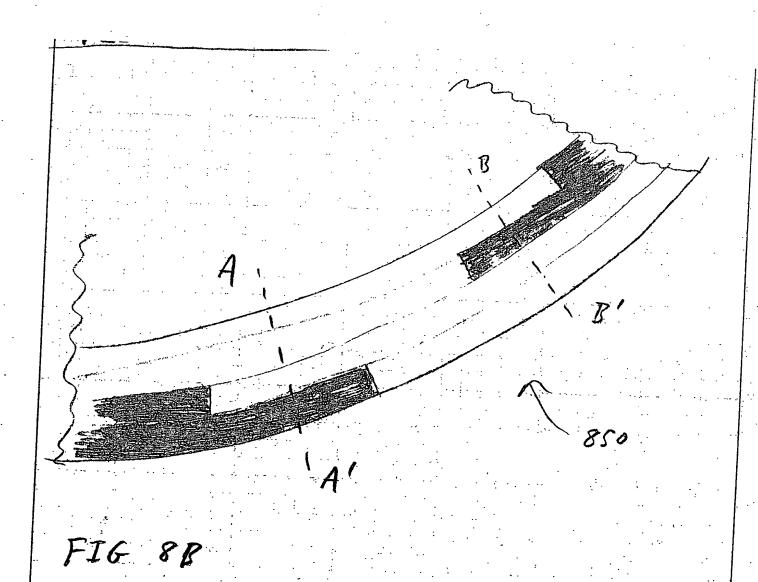


FIG 8A



Appln. No.: Not yet assigned Docket No.: SENS.008US3
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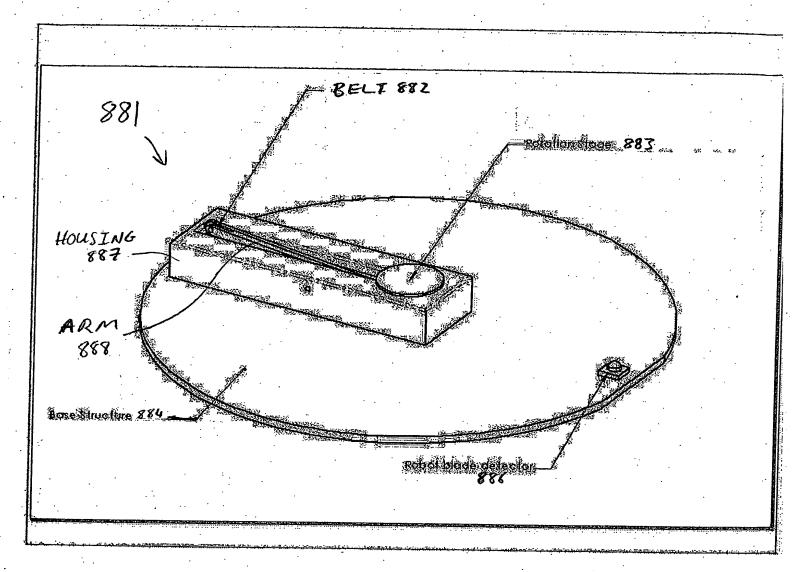
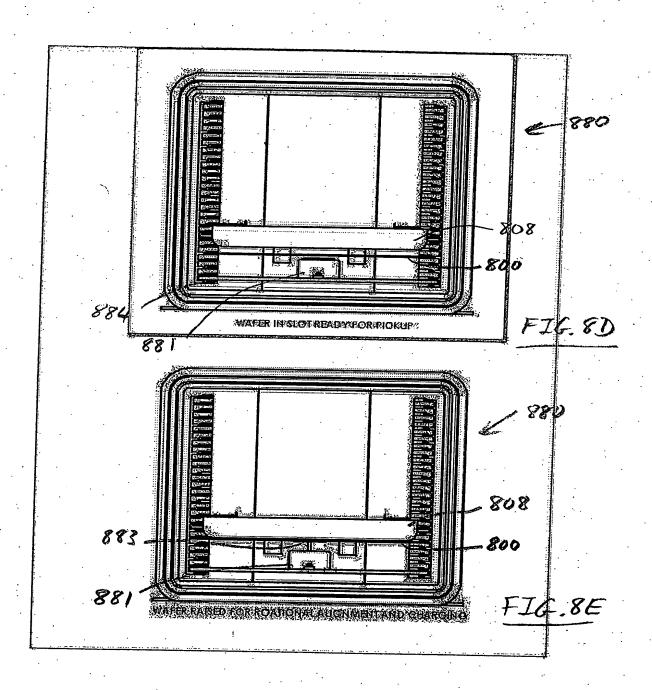


FIG8C

Inventors: Renken et al. v. Exp. Mail No.: EV 321 716 620 US Filing Date: November 21, 2003 Atty. Tel: (415) 318-1160

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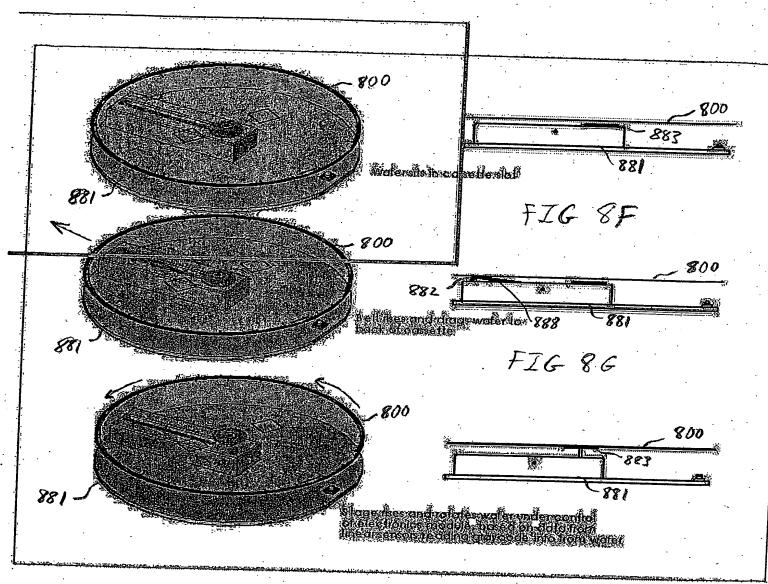


FIG 8H

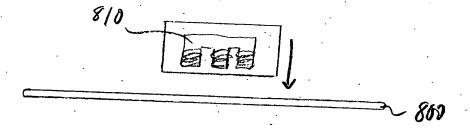


FIG 8I

